IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) An emulator circuit provided on one or more circuit boards of a circuit emulator, comprising:

a first programmable logic device configured to emulate a first partition of a circuit, and a second programmable logic device configured to emulate a second partition of the circuit, said first programmable logic device having pins configurable for providing output signals and said second programmable logic device having pins configurable for receiving input signals;

a serializer, coupled to said pins of said first programmable logic device, receiving said output signals from said first programmable logic device and providing a serialized data stream;

a cross point switch receiving said serialized data stream at a first input/output pin of said cross point switch and routing said data stream onto a second input/output pin of said cross point switch; and

a deserializer, coupled to said second input/output pin of said cross point switch and said pins of said second programmable logic device, receiving said data stream from said cross point switch and deserializing said data stream onto said pins of said second programmable logic device as said input signals.

2. (Original) An emulator circuit as in Claim 1, wherein selected pins on each programmable logic device are configured to receive input signals and to provide output signals, and wherein said signals on said selected pins of each programmable logic device are serialized and deserialized by a serializer/deserializer integrated circuit.

3. (Currently Amended) An emulator including the emulator circuit of Claim 1, said emulator comprising:

a circuit partitioner for synthesizing the first circuit partition and the second circuit partition from ~~a user~~the circuit ~~a first circuit partition and a second circuit partition~~; and

a configurer configuring (a) said first circuit partition in said first programmable logic device and said second circuit partition in said second programmable logic device, and (b) said cross point switch for routing said data stream between said first input/output pin and said second input/output pin.

4. (Original) An emulator as in Claim 3, wherein said configurer further configures said first and second programmable logic devices to provide virtual interconnections between said first and second circuit partitions.

5. (Original) An emulator as in Claim 3, wherein said configurer further configures said first and second programmable logic devices to provide a dedicated signal path to each input/output signal of said first and second circuit partitions.

6. (Original) An emulator as in Claim 3, wherein said configurer configures said cross point switch for static operations.

7. (Original) An emulator as in Claim 3, wherein said configurer configures said cross point switch for dynamic operations.

8. (Previously Presented) A method, comprising:

synthesizing from a user circuit a first circuit partition and a second circuit partition;

configuring said first circuit partition in a first programmable logic device and said second circuit partition in a second programmable logic device, said configuring providing output signals of said first circuit partition designated for said second circuit partition as output signals of the first programmable logic device, and providing input signals of said second circuit partition as input signals to said second programmable logic device;

serializing said output signals of said first programmable logic device to provide a serialized data stream;

configuring a cross point switch to route said serialized data stream from a first input/output pin of said cross point switch onto a second input/output pin of said cross point switch; and

deserializing said data stream from said cross point switch as said input signals of said second programmable logic device.

9. (Original) A method as in Claim 8, wherein said first and second programmable logic devices are each configured to receive input signals and to provide output signals, and wherein said serializing and deserializing of signals of each of said first and second programmable logic devices are carried out by a serializer/deserializer integrated circuit.

10. (Original) A method as in Claim 8, wherein said configuring provides in said first and second programmable logic devices virtual interconnections between said first and second circuit partitions.

11. (Original) A method as in Claim 8, wherein said configuring provides in said first and second programmable logic devices a dedicated signal path for each input/output signal of said first and second circuit partitions.

12. (Original) A method as in Claim 8, wherein said configuring of said cross point switch configures said cross point switch for static operations.

13. (Original) A method as in Claim 8, wherein said configuring of said cross point switch configures said cross point switch for dynamic operations.

14. (Previously Presented) An emulator circuit, comprising:

a first programmable logic device configured to emulate a first partition of a circuit and a second programmable logic device configured to emulate a second partition of the circuit, wherein (a) said first programmable logic device includes a serializer, configurable to receive output signals from a user circuit configurable on said first programmable logic device and to serialize said output signals to provide a data stream on an input/output pin of said programmable logic device, and (b) said second programmable logic device includes a deserializer configurable to receive said serialized data stream from an input/output pin of said second programmable logic device and to deserialize said data stream as input signals to a user circuit configurable on said second programmable logic device; and

a cross point switch receiving said data stream from said input/output pin of said first programmable logic device at a first input/output pin of said cross point switch and configurable to route said data stream onto a second input/output pin of said cross point switch coupled to said input/output pin of said second programmable logic device.

15. (Currently Amended) An emulator including the emulator circuit of Claim 14, said emulator comprising:

a circuit partitioner for synthesizing the first circuit partition and the second circuit partition from ~~a user~~the circuit ~~a first circuit partition and a second circuit partition~~; and

a configurer configuring (a) said first circuit partition in said first programmable logic device and said second circuit partition in said second programmable logic device, and (b) said cross point switch for routing said data stream between said first input/output pin and said second input/output pin.

16. (Original) An emulator as in Claim 14, wherein said configurer further configures said first and second programmable logic devices to provide virtual interconnections between said first and second circuit partitions.

17. (Original) A emulator as in Claim 14, wherein said configuring provides in said first and second programmable logic devices a dedicated signal path for each input/output signal between said first and second circuit partitions.

18. (Original) An emulator as in Claim 14, wherein said configurer configures said cross point switch for static operations.

19. (Original) An emulator as in Claim 14, wherein said

configurer configures said cross point switch for dynamic operations.

20. (Previously Presented) A method, comprising:

synthesizing from a user circuit a first circuit partition and a second circuit partition;

configuring said first circuit partition in a first programmable logic device and said second circuit partition in a second programmable logic device, said configuring includes providing a serializer in said first programmable logic device for serializing output signals of said first circuit partition designated for said second circuit partition as a serialized data stream provided on an input/output pin of said first programmable logic device, and providing a deserializer in said second programmable logic device to deserialize said serialized data stream received at an input/output pin of said second programmable logic device as input signals of said second circuit partition; and

configuring a cross point switch to route said serialized data stream from a first input/output pin of said cross point switch coupled to said input/output pin of said first programmable logic device onto a second input/output pin of said cross point switch coupled to said input/output pin of said second programmable logic device.

21. (Original) A method as in Claim 20, wherein said configuring provides in said first and second programmable logic devices virtual interconnections between said first and second circuit partitions.

22. (Original) A method as in Claim 20, wherein said configuring provides in said first and second programmable logic devices a dedicated signal path for each input/output signal between said first and second circuit partitions.

23. (Original) A method as in Claim 20, wherein said configuring of said cross point switch configures said cross point switch for static operations.

24. (Original) A method as in Claim 20, wherein said configuring of said cross point switch configures said cross point switch for dynamic operations.